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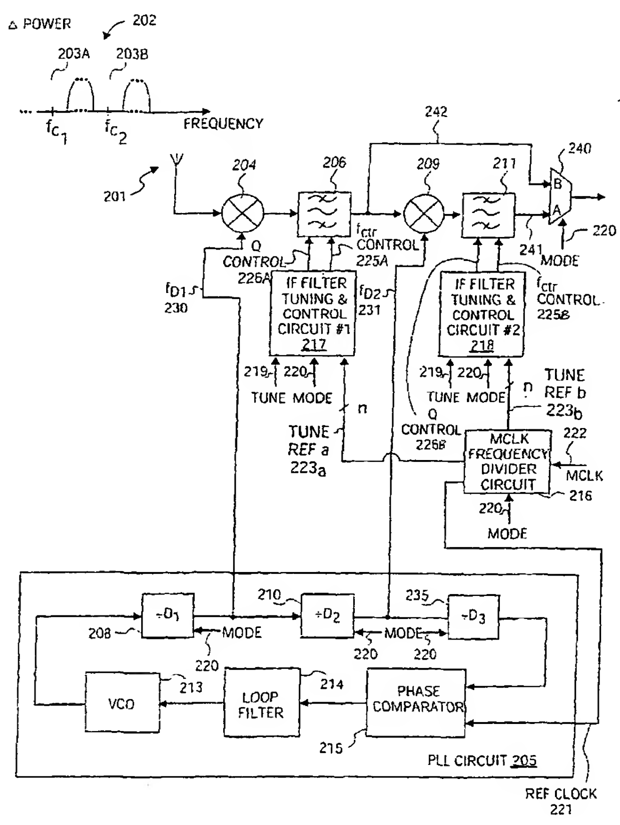
(54) **Title:** A GPS AND CELLULAR RECEIVER AND A METHOD FOR TUNING AND CONTROLLING ITS IF FILTER



(57) Abstract: A wireless receiver is described having an intermediate frequency (IF) filter that helps the wireless receiver receive a GPS wireless signal or a cellular wireless signal. The wireless receiver also has an IF filter tuning and control circuit that tunes and controls a passband characteristic for the IF filter in response to a mode input that indicates whether the GPS wireless signal or the cellular wireless signal is to be received. The IF filter tuning and control circuit is tailored to use a plurality of reference frequencies for the tuning of the IF filter. The IF filter tuning and control circuit also has an output that provides: 1) a first control signal to the IF filter so that the IF filter is tailored to receive the GPS wireless signal; and 2) a second control signal to the IF filter so that the IF filter is tailored to receive the cellular wireless signal.

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A Wireless Receiver and a Method of Determining a Change to a GPS Nominal Value

The present application hereby claims the benefit of the filing date of a related U.S. Provisional Application filed on January 23, 2001, and assigned Application Serial No. 60/263,808.

Field of the Invention

The field of invention relates generally to wireless communication; and, more specifically, to a method and apparatus for a GPS/cellular receiver having adaptive filtering that can be tuned with a plurality of frequency references.

Background

Referring to Figure 1, a portion 102 of the airborne electromagnetic power spectra that exists proximate to a receiving antennae 101 may be viewed as carrying a plurality of various radio signals and/or other transmitted wireless information. A desired portion 103 of the spectra 102 (e.g., a specific radio signal 103 from a particular transmission source) is typically "carried" over the airborne medium at a specific carrier frequency "fc".

That is, a specific wireless signal 103 to be received may be viewed as being "carried" across the airborne medium at its particular carrier frequency fc. Carrier frequencies are typically high frequencies (e.g., within the Radio Frequency (RF) band). For example, Global Positioning Satellite (GPS) signal carrier frequencies are commonly designed to be either 1.57542 GHz (for the L1 band) or 1.22760 GHz (for the L2 band); Code Division Multiplexed Access (CDMA) signal carrier receive frequencies are typically designed to be within a range of 869.0 to 894.0 MHz/1830.0 to 1900.0 MHz; and Advanced Mobile Phone System (AMPS) signal carrier receive frequencies are typically designed to be within a range of 869.0 to 894.0 MHz.

A wireless receiving device properly receives desired information from the airborne medium by focusing its signal processing operations upon the desired portion 103.

Because processing signals at high frequencies is typically more expensive than processing signals at low frequencies (e.g., from the perspective of the cost of the component(s) used to perform the processing), a signal processing technique referred to as "downconversion" is typically used to help focus the signal processing operations (mentioned just above) in a cost effective fashion.

That is, downconversion shifts the desired signal portion 103 from its high carrier frequency fc to a lower "intermediate frequency" f_{IF}. Mixing is typically used to implement downconversion and involves the multiplication of a received signal (e.g., the electromagnetic spectra 102) with a downconversion signal that acts as a frequency reference (e.g., a sinusoidal waveform). When the received signal and downconversion signal are multiplied a pair of resultant signals are created: 1) a first signal that may be viewed as the received signal being frequency shifted "downward" by an amount equal to the frequency of the downconversion signal (referred to as the subtractive term signal); and 2) a second signal that may be viewed as the received signal being frequency shifted "upward" by an amount equal to the frequency of the downconversion signal (referred to as the additive term signal).

For example, referring to Figure 1, a first mixer 104 multiplies the received electromagnetic spectra 102 with a first downconversion signal (that is provided by a phase lock loop circuit 105 at the output of a first feedback frequency divider 108). The first downconversion signal is designed to have a frequency of f_{D1}. As a result of the multiplication performed by the mixer 104, a pair of signals are created: 1) a subtractive term signal that may be viewed as the electromagnetic spectra 102 being frequency shifted "downward" by f_{D1} (which corresponds to the desired portion 103 having a carrier frequency equal to $fc-f_{D1}$); 2) an additive term signal that may be viewed as the electromagnetic spectra 102 being frequency shifted "upward" by f_{D1}.

A first intermediate frequency (IF) filter 106 receives both the additive and subtractive term signals but is designed to substantially pass only the desired portion within the subtractive term signal. The content of the first intermediate filter 106 output signal 107 can be configured to be only (approximately) the desired portion 103 carried at a

lower, first intermediate frequency f_{IF1} (where f_{IF1} = fc $-f_{D1}$) by designing the first IF filter 106 to have a passband: 1) centered proximate to the first intermediate frequency f_{IF1}; and 2) having a spectral width that is approximately coextensive with the spectral width Wr of the desired portion 103 within the received electromagnetic spectra 102.

As such, the output of the first IF filter 106 may be viewed as substantially the same as the content of the desired portion 103 but having a lower carrier frequency of f_{IF1} (rather than fc). As just one example, if desired portion 103 corresponds to GPS information carried in the L1 band (such that fc= 1.57542 GHz and the first downconversion signal has a frequency f_{D1} = 1.000 GHz, the output of the first IF filter 106 will correspond to the desired portion 103 having a reduced carrier frequency f_{IF1} = fc $-f_{D1}$ = 1.57542 – 1.000 = 0.57542GHz. In this manner, the receiver has "focused" its signal processing attention to just the desired portion 103 of information and has lowered its carrier frequency (e.g., so that less expensive components may be used to perform subsequent signal processing).

Note that a first feedback frequency divider 108 within a PLL circuit 105 may be configured to craft the frequency f_{D1} of the first downconversion signal. For example, if the PLL circuit 105 is designed to create a signal at the Voltage Controlled Oscillator (VCO) 113 output having a frequency of 2.000 GHz, the first downconversion signal frequency f_{D1} may be designed to be 1.000 GHz (as described in the example just above) by setting the frequency division D1 of the first frequency divider 108 to be 2.0. As such, the first frequency divider 108 accepts a 2.000 GHz signal and divides its frequency by 2.0 to produce a 1.000 GHz signal.

The f_{IF1} intermediate carrier frequency of the desired portion (observed at the output of the first IF filter 106) may be even further reduced via a second downconversion sequence. For example, as seen in Figure 1, a second mixer 109 multiplies the output signal 107 of the first IF filter 106 with a second downconversion signal having a frequency of f_{D2} (that is provided at the output of a second feedback frequency divider 110 within the PLL circuit 105). As such, the subtractive term signal at the output of

the second mixer 109 may be viewed as the desired portion 103 having a carrier frequency of $f_{IF2} = f_{IF1} - f_{D2}$.

For example, continuing with the exemplary design discussed so far, if the frequency division performed by the second frequency divider 110 is also 2.0, the second downconversion frequency f_{D2} will be 500 MHz because 1.000 GHz (which is the output frequency of the first frequency divider 108) divided by 2.0 is equal to 0.500 GHz = 500 MHz. As such, desired portion 107 will be downconverted to a second, lower intermediate frequency $f_{IF2} = f_{IF1} - f_{D2} = 575.42\text{MHz} - 500\text{MHz} = 75.42$ MHz.

Thus, by designing the second IF filter 111 to have a passband characterized by a center frequency proximate to f_{IF2} and a spectral width of Wr, the second IF filter 111 output signal 112 will correspond to only the desired portion 103 of the received electromagnetic spectra 102 having a significantly reduced carrier frequency of f_{IF2} (rather than fc). Note that the reference clock 121 input to the PLL circuit 105 will have a frequency of 500MHz because the PLL (with a total frequency division of 4.0 in its feedback path) is designed to multiply the reference clock input 121 signal frequency by 4.0 up to 2.000 GHz at the VCO 113 output.

As wireless information becomes ubiquitous, large commercial demand is expected for those receivers having the ability to receive different types of wireless signals (e.g., GPS, AMPS or CDMA). Tailoring a receiver to properly receive different types of wireless signals, however, raises challenges to the engineers responsible for a receiver's design.

Drawings

The present invention is illustrated by way of example, and not limitation, in the Figures of the accompanying drawings in which:

Figure 1 shows a dual downconversion stage for a wireless receiver.

Figure 2 shows an embodiment of a downconversion stage for a wireless receiver that can receive GPS, CDMA or AMPS wireless signals.

Figure 3a shows exemplary settings for the downconversion stage of Figure 2.

Figure 3b shows an embodiment of specific exemplary settings for the downconversion stage of Figure 2.

Figure 4a shows an exemplary passband for a second order IF filter.

Figure 4b shows an embodiment of a GmC filter design for a second order bandpass IF filter such as the second order bandpass IF filter shown in Figure 4a.

Figure 5a shows an embodiment of an IF Filter Tuning and Control circuit that may be used for tuning/controlling an IF filter that receives GPS, CDMA or AMPS wireless signals.

Figure 5b shows an embodiment of a sample and hold circuit that may be used for the sample and hold circuit shown in Figure 5a.

Figure 6a shows another embodiment of an IF Filter Tuning and Control circuit that may be used for tuning/controlling an IF filter that receives GPS, CDMA or AMPS wireless signals.

Figure 6b shows an embodiment of a sample and hold circuit that may be used for the sample and hold circuit shown in Figure 6a.

Description

Recall from the discussion in the background that challenges may arise if a receiver is designed to be capable of receiving different types of wireless signals. For example, commercial demand is anticipated for a wireless receiver that can receive a GPS signal

within various cellular environments such as GSM, CDMA and/or AMPS signals. Figure 2 shows an embodiment of a dual downconversion stage for a wireless receiver that can receive GPS information within the cellular environments of GSM, CDMA or AMPS.

Generally, the design of a receiver's downconversion involves two main obstacles: 1) the setting of the downconversion frequencies and IF filter passband characteristics; and 2) the tuning of the IF filter. Aspects of these challenges are discussed in the following description. A first subsection entitled "Downconversion and IF Filter Settings" will be followed by a second subsection entitled "IF Filter Tuning".

Downconversion and IF Filter Settings

A challenge with respect to the settings of the downconversion frequencies arises from the various carrier frequencies that may be used to carry the different types of wireless signals that the receiver is designed to receive. For example, recall from the background that Global Positioning Satellite (GPS) signal carrier frequencies are designed to be either 1.57542GHz (for the L1 band) or 1.22760 GHz (for the L2 band); Code Division Multiplexed Access (CDMA) signal carrier frequencies are designed to be within a range of 869.0 to 894.0 MHz/1830.0 to 1900.0 MHz; and Advanced Mobile Phone System (AMPS) signal carrier receive frequencies are designed to be within a range of 869.0 to 894.0 MHz.

Some of these different carrier frequency ranges are shown symbolically in Figure 2 where, within the airborne electromagnetic spectrum 202: 1) possible desired portion 203a may be viewed as having a carrier frequency fc1 that is located within a frequency range of 869.0 to 894.0 MHz (and is therefore associated with a cellular wireless signal type such as AMPS or CDMA); and 2) possible desired portion 203b may be viewed as having a carrier frequency fc2 that is located at 1575.24MHz and is therefore associated with GPS.

A receiver designed to properly receive a signal carried within any of the above described carrier frequency ranges should be able to generate downconversion signals

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having suitable downconversion frequencies f_{D1}, f_{D2} and IF filter 206, 211 characteristics (e.g., passband center frequency and passband spectral width) for receiving the wireless signal. As such, the receiver of Figure 2 is designed to change its downconversion frequencies f_{D1}, f_{D2} and IF filter characteristics in light of the type of wireless signal being received.

With regard to the exemplary depiction of Figure 2, these changes are triggered by changes in the "mode" input 220 of the receiver. The mode input 220 is observed in the following seven locations within the embodiment of Figure 2: 1) the first feedback frequency divider 208; 2) the second feedback frequency divider 210; 3) the third feedback frequency divider 235; 4) a first IF Filter Tuning and Control circuit 217 (that tunes and controls the center frequency and passband of a first IF filter 206); 5) a second IF Filter Tuning and Control circuit 218 (that tunes and controls the center frequency and passband of a second IF filter 206); 6) a master clock frequency divider circuit 216 that determines the frequency of a reference clock REF CLK 221 (and tuning reference signals Tune Ref_a 223a, and Tune Ref_b 223b); and 7) a multiplexer 240 that selects the output from either the first intermediate filter 206 or the second intermediate filter 211.

The multiplexer 240 allows the downconversion process to be either a "single" downconversion process (in which the received electromagnetic spectrum is downconverted only once via mixer 204) or a "dual" downconversion process (in which the received electromagnetic spectrum is downconverted twice via mixers 204 and 209). That is, if channel A is selected, dual downconversion is enabled; or, if channel B is selected, single downconversion is enabled.

Figure 3a shows at a high level how the different reception modes of the receiver can be entertained. A first mode, which may be referred to as the "GPS mode" (where a GPS signal is to be received), triggers a combination of receiver settings that are serially listed in the first row 301a of Figure 3a. A second mode, which may be referred to as the "cellular mode" (e.g., where an AMPS signal or CDMA signal is to be received), triggers a combination of receiver settings that are serially listed in the second row 302a

of Figure 3a. As AMPS signals and CDMA signals (and even GSM signals) can share a common spectral range (e.g., 869.0 to 894.0 MHz), in various embodiments, the combination of receiver settings used to receive these signals may share a large degree of overlap.

Different demodulation techniques downstream from the multiplexer 240 can be used to differentiate these signals so that a particular type of cellular signal can be successfully received. Referring to Figures 2 and 3a, each mode can be realized with a different mode input 220 value. As such, a change in the receiver's mode input 220 corresponds to a change in the type of signal to be received (e.g., GPS or cellular) and causes a string of changes in the receiving characteristics of the receiver.

For example, note that the downconversion signal frequencies f_{D1} 230, 330a and f_{D2} 231, 331a may be determined by setting the reference clock 221, 321a frequency and the feedback frequency divider 208, 308a, 210, 310a, 235, 335a values (which determine the multiplication 305a of the reference clock 221, 321a frequency that is performed by the PLL circuit 205). As seen in Figures 2 and 3a, the mode input 220 adjusts the master clock frequency divider circuit 216 value (which are listed as D3a and D3b in the first column 316a of Figure 3a for each mode). Thus, for a fixed master clock 222 frequency of Z MHz, the reference clock 221, 321a frequency for each mode (which is listed as f_{REFa} and f_{REFb} in the second column 321a of Figure 3a) may be expressed as Z/D3a for the GPS mode, and Z/D3b for the cellular mode.

Figure 3b shows a specific embodiment that conforms to the approach of Figure 3a. That is, Figure 3b shows an embodiment where specific values for each of the parameters listed in Figure 3a have been "filled out" so as to provide a working set of values for a combined GPS/Cellular receiver. Note that the embodiment of Figure 3b employs a common reference clock 221, 321b frequency of 0.2 MHz for each wireless signal type. That is, referring to Figure 3b, the master clock 222 frequency is Z=13.0 MHz for both modes and the master clock frequency divider circuit 216 value 316b is 65.0 for both modes. As such, the reference clock frequency is 13.0MHz/65.0 = 0.2 MHz and the mode input 220 to the master clock frequency divider circuit 216 can be

viewed as being unnecessary (at least for generation of the reference clock 221 frequency). Other embodiments as suggested by Figure 3a, however, can be designed to have "mode-dependent" reference clock frequency values f_{REFa}, f_{REFb}.

Because of the different carrier frequencies associated with the different modes, each combination of feedback frequency divider 208, 210, 235 values 308b, 310b, 335b particularly helps the downconversion process for the corresponding type of wireless signal to be received. Figure 3b shows an embodiment of the different downconversion frequencies 330b, 331b that may be used for each mode. Note that according to the particular embodiment of Figure 3b, dual downconversion is used for both GPS mode and cellular mode.

As such, the channel A input of multiplexer 240 of Figure 2 is enabled for both modes (which means that, alternatively, the multiplexer 240 may be removed). In alternate embodiments, however, single downconversion may be used for both modes (in which case the second mixer 209 and the second IF filter 211 may be removed); or, single downconversion may be used for one mode but dual downconversion may be used for another mode (in which case the multiplexer 240 becomes useful).

Referring to Figures 2 and 3a, the multiplication of the reference clock 221, 321a frequency as performed by the PLL circuit 205 may be expressed as the total division performed along its feedback path. As such, the frequency multiplication performed by the PLL circuit 205 for each mode (which is shown in column 305a of Figure 3a) may be expressed as Xa = D1aD2aD3a for the GPS mode; and Xb = D1bD2bD3b for the cellular mode. According to the specific embodiment of Figure 3b, as seen in columns 308b, 310b, and 335b, the feedback divider values D1a, D2a, D3a for the GPS mode are 2.0, 42.0 and 16096/84 (where 16096/84 □ 191.619) which results in a PLL multiplication value (as seen in column 305b) of 16096 (i.e., 2x42x191.619 □ 16096.0). Thus, for a 0.2 MHz reference clock value 321b, a VCO 213 output signal frequency value 313b of 3219.2 MHz results.

The downconversion frequencies and IF frequencies that result from the specific feedback division in the PLL feedback path can be observed in Figure 3b. Note that the GPS carrier frequency is assumed to be 1575.4 MHz such that a first downconversion frequency value 330b of 1609.6 MHz produces a first IF frequency value 304b of 34.18 MHz (i.e., 1609.6 MHz – 1575.4 MHz = 34.2 MHz). A similar analysis as that described above can be performed for the cellular mode found in the second row of the table shown in Figure 3b.

Note that, in the embodiment of Figure 3b, each feedback divider 208, 210, 235 performs a first frequency division for the GPS mode and a second frequency division for the cellular mode (e.g., the first feedback divider 208 performs a division of 2.0 for GPS mode and 1.0 for cellular mode). Frequency dividers can be commonly implemented in logic as counter-like circuits that trigger an output signal edge after a certain number of input signal edges have been observed. In an embodiment, within a logic divider, a unique count value is used for each mode input value 220 to trigger an output signal edge (which corresponds to a unique frequency division value for each mode). Thus changes in frequency division can be easily configured on a "per-mode" basis.

Note also that non-integer frequency division is also possible (e.g., as exhibited by the third feedback divider 235). As cellular communications also typically involve a plurality of individual channels within an electromagnetic spectra region (wherein each channel has its own associated frequency), a feedback divider can be designed to be able to further resolve the frequency division it performs (e.g., via non integer frequency division) so that a specific channel may be received. As such, for example, the third feedback divider 235 may be responsive to a signal representative of a particular channel to be received instead of (or in combination with) the mode input 220. Thus, as just one example, the first a second feedback division values may remain constant in cellular mode (e.g., 1 and 4.3 respectively as seen in Figure 3b) but the third feedback division value 335b varies within the cellular mode so that particular channels can be received.

To summarize the scope of the discussion so far, a receiver designed to receive GPS or cellular (e.g., AMPS or CDMA) signals may be configured to generate different sets of feedback divider values (e.g., D1a or D1b for the first feedback divider 208; and/or, D2a or D2b for the second feedback divider 210) for each of these wireless signal types. The unique "per mode" set of feedback divider values result from an effort to make the receiver responsive to the different ranges of carrier frequencies that exist for the different types of wireless signals that may be received.

Before continuing, it is important to point out that the specific values listed in Figure 3b are exemplary and constitute just one embodiment. Various other combinations of master clock frequency, reference clock frequency, feedback division, downconversion frequency and intermediate frequency can be determined by those of ordinary skill. Notably, however, for a reference clock frequency between 0.1 and 1.0 MHz and a VCO frequency between 1.0 and 4.0 GHz, PLL multiplication values should be within a range of 1,000 to 40,000. Furthermore, to the extent that the reception of signals from a plurality of carrier frequencies may be desirable within a particular mode, those of ordinary skill will be able to add additional combinations of receiver settings (e.g., as described just above with respect to the third feedback divider 235). Receiver settings for reception within other frequency spectra ranges (e.g., 1830.0 to 1900.0 MHz) can also be configured.

Continuing then, recall from the background that the passband characteristics of the IF filters 206, 211 are typically tailored in light of the intermediate frequencies and spectral widths that apply to a desired portion during its downconversion sequence. As discussed, an intermediate frequency is a function of the difference between a desired portion's carrier frequency and its downconversion frequency. The spectral width may be viewed as a function of the desired portion's applicable modulation technique, industry standard and/or governmental regulation.

In light of these factors, the receiver embodiment of Figure 2 is also designed to establish a unique set of IF filter 206, 211 passband characteristics for each of the wireless signal types the receiver may receive. The receiver embodiment of Figure 2 is

therefore designed to include a pair of IF Filter Tuning and Control circuits 217, 218 that control and tune the IF filter 206, 211 passband characteristics, respectively, in light of the mode input 220 value. The IF filter Tuning and Control circuits 217, 218 not only establish their corresponding IF filter 206, 211 characteristics in light of the mode input 220 value (e.g., during normal operation of the receiver) but also "tune" their corresponding IF filters 206, 211 (e.g., during manufacturing of the receiver or a wireless device that incorporates the receiver) so that inaccuracies associated with manufacturing and/or environmental tolerances may be canceled, reduced or otherwise compensated for.

The *following discussion will elaborate firstly on techniques that may be used to* establish different sets of IF filter 206, 211 passband characteristics, for each receiver mode, during normal operational usage of the receiver (e.g., "after manufacturing"). This first discussion will be followed by a second discussion that elaborates on techniques that may be used to "tune" these different sets of IF filter characteristics beforehand (e.g., "during manufacturing") so that manufacturing and/or environmental tolerances may be accounted for.

As discussed, the passband of an IF filter may be characterized by: 1) its center frequency f_{ctr}; and 2) its spectral width W. Figure 4a shows an exemplary passband for a second order IF filter. Figure 4a shows the general shape of a second order filter passband H(s) 401, its center frequency f_{ctr} 402 and its spectral width W 403. Note that, according to one approach, the spectral width W 403 may be referenced to its –3.0 dB point (i.e., the point where signal amplitude drops by a factor of 2.0 as compared to signal amplitude at the center frequency f_{ctr} 402).

Another spectral width parameter, referred to as the Q factor, may be defined as the center frequency f_{ctr} 402 normalized by the spectral width W 403 (i.e., $Q = f_{ctr}/W$). The Q factor is typically used to describe a passband filter because of the way different filter component values affect the shape and position of the passband H(s) 401. That is, a *change in a bandpass filter component value may not only affect its spectral width* W 403 but may also affect its center frequency fctr 402.

Figure 4b shows an embodiment of a GmC filter design for a second order bandpass IF filter 406 such as the second order bandpass IF filter described in Figure 4a. A GmC filter, according to various embodiments, uses a combination of transconductance amplifiers 404, 405, 407,, 408 (which convert an input voltage into an amplified output current) and capacitances C1, C2 to establish a second order bandpass shape H(s) 401 as well as a particular center frequency 402, spectral width W 403 and Q factor.

Referring to the equations shown in Figure 4b, note that the gain Gm3, Gm4 of transconductance amplifiers 407, 408 may be used to control the center frequency f_{ctr} 402 of the IF filter 406 (i.e., f_{ctr} = ((Gm3Gm4/C1C2)*0.5)/2pi. Furthermore, once the center frequency f_{ctr} 402 of the IF filter 406 has been established by setting the Gm3 and Gm4 values, the gain Gm2 of transconductance amplifier 405 may be used to control the spectral width W 403 of the IF filter 406 (via manipulation of the Q factor).

As such, the IF filter 406 embodiment of Figure 4b possesses a pair of control inputs (Q factor control 426, and f_{ctr} control 425) that are used to manipulate the gain of their respective transconductance amplifiers 405, 407, 408 so that the passband characteristics of the IF filter 406 may be controlled. Specifically, in an embodiment, a control voltage applied to a control input (e.g., control input 425) determines the corresponding gain of the transconductance amplifer(s) (e.g., amplifiers 407, 408) coupled to the control input.

Referring back to Figure 2, as just an example, control input 225a to IF filter 206 (or control input 225b to IF filter 211) may be viewed as corresponding to the f_{ctr} control input 425 observed in Figure 4b; and, control input 226a to IF filter 206 (or control input 226b to IF filter 211) may be viewed as corresponding to the Q factor control input 426 observed in Figure 4b. As such, in an embodiment, the IF Tuning and Control circuit 217 supplies the aforementioned control voltage(s) to IF filter 206, in response to the mode input 220 value, so that IF filter 206 can implement different passband characteristics for each type of wireless signal to be received (e.g., a first set

of passband characteristics for GPS mode and a second set of passband characteristics for cellular mode).

Similarly, the IF Tuning and Control circuit 218 supplies the aforementioned control voltage(s) to IF filter 211, in response to the mode input 220 value, so that IF filter 211 can also implement different passband characteristics for each type of wireless signal to be received. Before continuing further, it is important to point out that alternate embodiments may employ IF filter technologies other than GmC type filters, other than 2nd order bandpass filters. Furthermore, filter passband characteristics other than center frequency or Q factor may be defined and/or controlled by a tuning and control circuit. As such, the teachings herein should not be construed as being limited solely to the exemplary embodiments shown in Figure 4a and 4b.

Figure 5a shows an embodiment of an IF Filter Tuning and Control circuit 517 (that may be used for either of the tuning and control circuits 217, 218 shown in Figure 2). The embodiment of Figure 5a may be used to supply either or both of the control 425, 426 inputs of Figure 4b. For example, the control output 525/526 may provide (e.g., as a partitioned signal) both the f_{ctr} control 425 value and the Q factor control 426 value (e.g., where the f_{ctr} control value is associated with a first partition and the Q factor control is associated with a second partition). Alternatively, a pair of tuning and control circuits 517 (or, a pair of sample and hold circuits 550a that are each coupled to the loop filter 502) may be combined in order to construct one of the tuning and control circuits of Figure 2 (such that a pair of control outputs are formed).

In order to account for any of these approaches, the output of the IF Filter Tuning and Control circuit of Figure 5a is depicted as control output 525/526 for convenience. Note that the IF Filter Tuning and Control circuit 517 includes a phase lock loop circuit (as embodied with a phase comparator 501, loop filter 502 and VCO 503) and a sample and hold circuit 550a. The phase lock loop circuit, as described in more detail below, is used for the "tuning" of the IF filter (e.g., during manufacturing) and, as such, does not need to apply during normal operational mode of the receiver (e.g., after manufacturing of the receiver or a wireless device that incorporates the receiver).

During normal operational mode, the sample and hold circuit 550a provides the proper control signal(s) (at control output 525/526) to the IF filter (e.g., to control the IF filters center frequency and/or Q factor). The sample and hold circuit 550a maintains a plurality of control signals and "looks to" the mode input 520 value to understand which control signal should be provided to the IF filter. As such, a particular control signal is supplied for a particular type of wireless signal to be received (which results in the establishment of specific IF filter characteristics for the particular type of wireless signal to be received). For example, a first control signal is applied in GPS mode (e.g., to set the appropriate center frequency for the GPS mode); and, a second control signal is applied in cellular mode (e.g., to set the appropriate center frequency in cellular mode).

Figure 5b shows an embodiment of a sample and hold circuit 550b that may be used for the sample and hold circuit 550a of Figure 5a. The Analog-to-Digital Converter (ADC) 551 and Central Processing Unit (CPU) 552 are used, as described in more detail below, during the tuning of the receiver. The multiplexer 554 and Digital-to-Analog Converters (DAC) 555a, 555b are used during the normal operational mode of the receiver. Registers R1 553a and R2 553b are used during both the tuning and the normal operational mode. Specifically, as described in more detail below, the proper control signals for the IF filter are stored into registers R1 553a and R2 553b during IF filter tuning.

That is, for example: 1) the digital representation of a first IF filter control voltage for the GPS mode is stored into register R1 553a; and 2) the digital representation of a second IF filter control voltage (e.g., for the cellular mode) is stored into register R2 553b. As such, during normal operational mode, if the mode input 520 value (which may be viewed as corresponding to mode input 220 of Figure 2) corresponds to the GPS mode, an analog representation (e.g., a voltage) of the digital content of register R1 553a is provided to multiplexer 554 by digital to analog converter (DAC) 555a. The value of the mode input 520 selects the output of DAC 555a as the output of multiplexer 554 (which corresponds to the control output signal 525/526).

As such, an appropriate analog control signal is sent to the IF filter for the GPS mode. In a similar manner, the appropriate analog control signal is provided at the control output 525/526 for the cellular mode (as derived from the contents of register R2 553b and DAC 555b). In alternate approaches the control output 525/526 can be digital (e.g., where a DAC is incorporated into the IF filter).

As mentioned above, a digital representation of the proper control signal (e.g., one n bit wide word having a binary value that indicates the appropriate analog voltage to be applied to the IF filter), for each mode, is stored into registers R1 553a and R2 553b during IF filter tuning. These digital representations are determined by the CPU unit 552. The CPU 552 may be constructed with digital circuitry or with a processor that executes software routines. The CPU 552 has access to a "nominal" control signal representation for each mode (e.g., within a non volatile memory such as a Read Only Memory (ROM)).

For example if the receiver is designed such that, during GPS mode, the center frequency of the IF filter is supposed to be 30.0 MHz – the CPU unit 552 will have access to a "nominal" control signal representation of a control signal (e.g., a control voltage or current) that properly positions the center frequency of the IF filter at 30.0 MHz. The nominal control signal representation may also be referred to as a nominal control value, a nominal value, and the like.

Provided inaccuracies in the IF filter (e.g., from manufacturing tolerances or environmental affects) are not detected, the nominal control value is employed and the IF filter center frequency is set at 30.0 MHz during normal operational mode. That is, the nominal control value is loaded into its appropriate register (e.g., the nominal control value for the GPS mode is stored into register R1 553a and the nominal control value for the cellular mode is stored into register R2 553b).

IF Filter Tuning

Due to manufacturing tolerances (such as inconsistent doping quantities) or environmental effects (such as temperature effects or supply voltage effects), however,

inaccuracies may arise in the performance of the IF filter components. The presence of such inaccuracies, if left uncorrected for, can result in the passband of the IF filter effectively "missing" the desired band of information (such as desired portion 203a as shown back in Figure 2) to be captured after its corresponding downconversion. If the IF filter "misses" the information to be captured, the viability of the wireless communication itself is jeopardized.

As such, the CPU unit 552 should also be provided with an indication of an inaccuracy within the IF filter should one exist. In an embodiment, the inaccuracy information is used by the CPU unit 552 to adjust the nominal value for the IF filter's center frequency setting and bandwidth setting in a direction that compensates or otherwise begins to correct for the detected inaccuracy.

For example, if the inaccuracy indication signifies that the center frequency position of the IF filter is greater than its "nominal" or "designed for" frequency, the CPU unit 552 stores a lower control value (as compared to the nominal control value that is maintained for the IF filter as discussed above) into the appropriate register for use during normal operational mode (e.g., a lowered GPS control value is stored into register R1 553a and a lowered cellular control value is stored into register R2 553b). When used during normal operational mode, the lowered control value effectively positions the IF filter center frequency at its correct location so that the desired band of information is captured.

As described in more detail below, reference elements that are constructed out of circuit structures that are similar to those used to construct the IF filter(s) are used to provide an indication of an inaccuracy. These reference elements usually take two forms, either a PLL with the VCO constructed from the same circuit structure(s) as the IF filter; or with a monostable relaxation timing element. Both techniques employ a frequency reference signal (e.g., a reference clock) to tune the IF filter. For simplicity, the following discussion concerns a PLL based correlation technique but it should be understood that those of ordinary skill will be able to take the teachings herein and apply them to a monostable relaxation element approach.

With respect to the embodiments presented in Figures 5a and 5b, the inaccuracy indication is provided to the CPU unit by an analog-to-digital converter (ADC) 551 which provides a digital representation of the loop filter 502 output voltage. The loop filter 502, as shown in Figure 5a, is a component within a phase lock loop circuit that is configured to "lock onto" a reference frequency signal Tune Ref 523. The reference frequency signal Tune Ref 523 corresponds to the aforementioned frequency reference.

In an embodiment, the Tune Ref 523 signal is generated by a frequency divider circuit such as the MCLK frequency divider circuit 216 observed in Figure 2. As such, the Tune Ref 523 signal of Figure 5a may be viewed as either one of the Tune Ref signals 223_a or 223_b of Figure 2. In alternate embodiments, the frequency reference signal may be generated from the reference clock 221, the master clock 222 or another clock or frequency reference that can be made available to the wireless receiver.

By designing a "correlation" between the construction of the VCO 503 and the construction of the IF filter, as described in more detail below, the loop filter 502 output voltage will reflect the existence and extent of an IF filter inaccuracy (should one exist). The CPU unit 552 observes the loop filter 502 output voltage (via the ADC 551) and, if an IF filter inaccuracy is indicated, determines an appropriate modification to the IF filter's nominal control value in response (based upon an understanding of this correlation).

In an embodiment, the aforementioned correlation is implemented by: 1) designing the IF filter with a first element that sets an IF filter passband characteristic (e.g., the center frequency or Q factor); and, 2) designing the VCO 503 with a second element (referred to as a reference element) that sets the gain of the VCO 503 (as measured in Hz/volt). As such, a manufacturing defect or environmental condition that affects the first element (which causes an inaccuracy in the IF filter passband) should also similarly affect the second element (which causes a change in the gain of the VCO 503 away from its nominal design point).

In various embodiments, in order to enhance the correlation, the first element and reference element are the same type of circuit component (e.g., both elements are a resistor or both elements are a capacitor) or the same type of circuit design (e.g., both elements have a differential amplifier structure). An exemplary approach for tuning the center frequency of a GmC IF filter would include: 1) designing the IF filter such that a first resistor helps determine the gain of a transconductance amplifier that sets the IF filter's center frequency (such as transconductance amplifiers 405, 407, 408 of Figure 4b); and 2) designing the VCO 503 such that a second resistor (the reference element) is part of an RC load that affects inverter propagation delay within an "inverter ring" type VCO 503.

In the absence of any manufacturing or environmental induced inaccuracies, the IF filter center frequency will be positioned at its nominal center frequency (if the nominal value is applied at its center frequency control input 425). As a result of the IF filter/VCO correlation, the VCO 502 will possess its nominal gain which, in turn, will be reflected in the loop filter 502 output voltage settling to a value that corresponds to a nominal or "designed for" loop filter 502 output voltage. In this case, the CPU unit 552 can recognize (from the ADC 551) that the loop filter output voltage has settled to its nominal value. In response, the nominal control value for the IF filter center frequency may be placed into its corresponding register for each operating mode (e.g., the GPS nominal value may be placed into register R1 553a and the cellular nominal value may be placed into register R2 553b).

If a manufacturing or environmental induced inaccuracy arises, however, the responsible manufacturing defect or environmental condition will also cause a change in the gain of the VCO 503 away from its nominal value. As such, the VCO 503 will operate at a frequency other than its nominal operating frequency if the nominal loop filter 502 output voltage were to be applied to the input of the VCO 503. As the VCO 503 is forced to operate at the reference frequency according to basic PLL principles (because the PLL embodiment of Figure 5a does not posses feedback division), the loop filter 502 output voltage will deviate from its nominal value in order to compensate for the altered gain of the VCO 503.

That is, the loop filter 502 output voltage is expected to: 1) rise above its nominal value if the VCO 503 gain drops; or, 2) fall below its nominal value if the VCO 503 gain rises. The CPU unit 552 (via ADC 551) can detect the deviation of the loop filter 502 output voltage away from its nominal value so as to recognize that an manufacturing or environmental inaccuracy has been induced. Furthermore, the CPU unit 552 can "correct" the improper positioning of the center frequency of the IF filter passband based upon the extent to which the loop filter 502 voltage has deviated from its nominal value.

For example, in an embodiment where an increase in the IF filter center frequency corresponds to a decrease in the gain of the VCO 503, the CPU unit 552 will lower the IF filter center frequency in response to an observation that the loop filter 502 output voltage has risen above its nominal value. The CPU unit can lower the IF filter center frequency by changing (e.g., lowering) the nominal control value(s) that are maintained for each mode. The extent and direction that the nominal control value is modified (in light of the extent and direction of the observed deviation from the loop filter's 502 nominal output voltage) can be based upon a theoretical understanding of the design if the IF filter, the VCO 502 and the dynamics of the loop filter 502; and, as such, may vary from embodiment to embodiment.

Referring back to Figure 2, note that the Tune Ref signals 223a, 223b may be of multiple dimension "n". For example, the approach discussed above involved a case where a single frequency reference (Tune Ref 523) was used by an IF Filter tuning and control circuit 517a to tune its corresponding IF filter (i.e., n =1). Figure 6a, however, shows another embodiment wherein a pair of frequency references (Tune Ref_1 623_1 and Tune Ref_2 623_2) are used by an IF filter tuning and control circuit 617 to tune its corresponding IF filter (i.e., n=2). As such, whereas the IF filter tuning and control circuit 517 of Figure 5a used a single loop filter control voltage 516 (via a single PLL circuit), the IF filter tuning and control circuit 617 of Figure 6a uses a pair of loop filter control voltages 616_{1a}, 616_{2a} to tune its corresponding IF filter (alternatively, a single reference signal can be used whose frequency can be varied to a pair of frequencies).

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A pair of PLL circuits 601, 602, provide the pair of loop filter voltages 616_{1a}, 616_{2a} wherein loop filter voltage 616_{1a} is generated from the first PLL circuit's 601 attempt to "lock onto" the first reference frequency signal Tune Ref_1 623_1; and, loop filter voltage 6162a is generated from the second PLL circuit's 602 attempt to "lock onto" the second reference frequency signal Tune Ref_2 623_2. Using a pair of reference frequencies (via the pair of reference frequency signals 623_1, 623_2) allows for a wider tuning range and/or greater tuning accuracy.

As described with respect to Figure 5a and 5b, an IF filter within a receiver that can handle different wireless signal types (such as GPS and cellular) can be asked to reliably receive information at different passband characteristics (e.g., different center frequencies and Q factors). Using a pair of reference frequencies (e.g., via different reference frequency signals Tune Ref_1 623_1 and Tune Ref_2 623_2) allows for, at least, a separate frequency to be used to tune the IF filter at each of its unique operating modes. As such, multiple "test points" in the tuning process are possible.

For example, as just one approach, the Tune Ref_1 reference frequency signal 623_1 may be used to tune the IF filter for its GPS mode; and, the Tune Ref_2 reference frequency signal 623_2 may be used to tune the IF filter for its cellular mode. As these signals have different frequencies, a unique frequency is used to tune the IF filter for each operating mode.

Thus as an example, if the sample and hold circuit 550b of Figure 5b is employed, the control value stored in the R1 register 553a is based upon the observation of the first loop filter output voltage 616_{1a} (which is responsive to the frequency of the first reference frequency signal Tune Ref_1 623_1); and, the value stored in the R2 register 553b is based upon the observation of the second loop filter output voltage 616_{2a} (which is responsive to the frequency of the second reference frequency signal Tune Ref_2 623_2).

Note that the embodiment of Figure 6a employs a unique PLL circuit for each of the reference frequency signals Tune Ref_1 623_1 and Tune Ref_2 623_2 (which results in a pair of PLL circuits 601, 602). This allows tuning at different frequencies to occur simultaneously (i.e., loop filter output voltages 616_{1a} and 616_{2a} can be measured and analyzed at the same time). In alternate embodiments, a single PLL loop circuit may be used (e.g., as observed in Figure 5a) that is responsive to a single signal Tune Ref input 523. Here, however, the frequency of the signal that appears on the signal line 523 may be made to vary so that tuning measurements can still be made at different frequencies.

For example, the frequency of the signal that appears at the Tune Ref 523 input of Figure 5a may be configured to have: 1) over a first time period, a first frequency for a first tuning measurement (e.g., that helps to determine the appropriate content of register R1 553a of Figure 5b); and, 2) over a second time period, a second frequency for a second tuning measurement (e.g., that helps to determine the appropriate content of register R2 553b of Figure 5b). Here, although a plurality of reference frequencies are used, a single signal line 523 can be used to propagate the plurality of reference frequency signals.

In the approach described just above, note that although the MCLK frequency divider circuit 216 of figure 2 can supply as few as one reference signal (i.e., n =1 for Tune Ref signals 223a and 223b), the divider circuit 216 is responsible for providing different frequencies (e.g., via different division amounts) on a single reference signal line. The frequency divider circuit can supply a plurality of different Tune Ref signals that each have their own unique reference frequency.

In a related approach, the divider circuit 216 may be designed to supply only one frequency to an IF filter tuning and control circuit. That is, referring to Figure 5a, the frequency of the Tune_Ref input 523 signal remains constant. Here, different tuning frequencies can nevertheless be successfully employed by inserting a feedback divider between the VCO 503 and the phase comparator 501 whose division can be modified. By changing the feedback divider's division, a different VCO 503 output signal frequency will result. This will provide different loop filter control voltages which can

be used to support multiple "test points" for IF filter tuning as has been described. In still other embodiments, reference frequency signals may be derived from other frequency sources other than a common master clock MCLK.

The use of multiple "test points" in the IF filter tuning process allows the receiver to receive appropriate IF filter tuning over a wider frequency span (which is apt to be helpful if the same IF filter is expected to handle different wireless signal types) and/or more accurate tuning overall. For example, if the inaccuracy of an IF filter parameter (such as center frequency or Q factor) is non linear with respect to certain environmental or manufacturing effects (e.g., if a certain manufacturing result causes noticeable center frequency error at high frequencies but not at medium range frequencies), the appropriate "change" to be applied to each of the nominal control values may differ from operating mode to operating mode (e.g., the cellular nominal control value may be acceptable but the GPS nominal control value may need to be changed).

Using a plurality of reference frequencies to test/tune the IF filter therefore allows these non linearities to better understood, characterized and/or accounted for. So far, one embodiment has been described where a unique reference frequency is used to tune the IF filter for each operating mode (e.g., a first reference frequency for GPS, a second reference frequency for cellular, etc.). Still other embodiments are also possible. For example, a range of different Tune Ref signal frequencies may be applied (and the responsive loop filter voltage compared to an expected value) in order to map out manufacturing/environmental effects on the reference element across a wide frequency span.

For example, according to an "extrapolated" technique, a "test point" loop filter control voltage may be sampled for each of a plurality of reference frequencies (e.g., two or more) wherein each reference frequency is tailored so that each "test point" loop filter control voltage is less than (or greater than) the "nominal" loop filter control voltage for an IF filter mode. Based upon a theoretical or empirical understanding of the correlation between the reference element and the IF filter, the "test point" data can be

used to extrapolate the amount if error (if any) in the IF filter settings; and, calculate an appropriate correction to the nominal control value(s) in response.

According to another technique that may be referred to as "interpolated", a "test point" loop filter control voltage may be sampled for each of a plurality of reference frequencies (e.g., two or more) wherein the "nominal" loop filter control voltage for an IF filter mode is within the range of nominal "test point" loop filter control voltages (rather than being above or below them as in the extrapolated case). For example, in one case a pair of reference frequencies are applied whose corresponding control voltages produce one control voltage beneath the nominal control voltage and another control voltage above the nominal control voltage (i.e., the nominal control voltage is between the pair of test control voltages).

Again, based upon a theoretical or empirical understanding of the correlation between the reference element and the IF filter, the "test point" data can be used to interpolate the amount if error (if any) in the IF filter settings; and, calculate an appropriate correction to the nominal control voltage in response. Figure 6b shows an embodiment of a circuit that can be used for an interpolated approach wherein the nominal control voltage resides somewhere between a first test control voltage (e.g., which is applied at node 616_{1B}) and a second test control voltage (e.g., which is applied at node 616_{2B}).

The appropriate test control voltages are combined with resistances R1 and R2 to produce a voltage at the input of an ADC 651. In an embodiment, the settings of R1 and R2 are in proportion with the positioning of the nominal control voltage (e.g., if the nominal control voltage is designed to be midway between the pair of test control voltages, R1 may be set equal to R2). Other circuits are possible wherein each test control voltage is sampled (simultaneously or at separate times) and processed individually (rather than in a combined fashion as seen in Figure 6b).

Note also that embodiments of the present description may be implemented not only within a semiconductor chip but also within machine readable media. For example, the designs discussed above may be stored upon and/or embedded within machine readable

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media associated with a design tool used for designing semiconductor devices. Examples include a netlist formatted in the VHSIC Hardware Description Language (VHDL) language, Verilog language or SPICE language. Some netlist examples include: a behavioral level netlist, a register transfer level (RTL) netlist, a gate level netlist and a transistor level netlist. Machine readable media also include media having layout information such as a GDS-II file. Furthermore, netlist files or other machine readable media for semiconductor chip design may be used in a simulation environment to perform the methods of the teachings described above.

Thus, it is also to be understood that embodiments of this invention may be used as or to support a software program executed upon some form of processing core (such as the CPU of a computer) or otherwise implemented or realized upon or within a machine readable medium. A machine readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

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Claims

1. A wireless receiver, comprising:

a) an intermediate frequency (IF) filter that helps said wireless receiver receive a GPS wireless signal or a cellular wireless signal; and

b) an IF filter tuning and control circuit that tunes and controls a passband characteristic for said IF filter in response to a mode input that indicates whether said GPS wireless signal or said cellular wireless signal is to be received, said IF filter tuning and control circuit tailored to use a plurality of reference frequencies for said tuning of said IF filter, said IF filter tuning and control circuit having an output that provides: 1) a first control signal to said IF filter so that said IF filter is tailored to receive said GPS wireless signal; and 2) a second control signal to said IF filter so that said IF filter is tailored to receive said cellular wireless signal.

2. The wireless receiver of claim 1 wherein said cellular wireless signal can be an AMPS signal.

3. The wireless receiver of claim 1 wherein said cellular wireless signal can be a CDMA wireless signal.

4. The wireless receiver of claim 1 wherein said cellular wireless signal can be a GSM wireless signal.

5. The wireless receiver of claim 1 further comprising a mixer that provides a downconverted wireless signal to said IF filter.

6. The wireless receiver of claim 5 further comprising a phase lock loop circuit having a first feedback frequency divider that provides a first downconversion signal to said mixer, said phase lock loop circuit having a second feedback frequency divider that provides a second downconversion signal to a second mixer, said phase lock loop circuit tailored to multiply the frequency of reference clock in response to said mode signal.

7. The wireless receiver of claim 1 further comprising a frequency divider that divides the frequency of a second clock signal to provide said reference clock.

8. The wireless receiver of claim 7 wherein said reference clock frequency is less than 1 MHz.

9. The wireless receiver of claim 7 wherein said second clock frequency is 13.0 MHz.

10. The wireless receiver of claim 1 wherein said PLL circuit further comprises a third feedback frequency divider.

11. A wireless receiver, comprising:

a) a first mixer and a first intermediate frequency (IF) filter that receives an output signal from said first mixer;

b) a second mixer that receives an output signal from said first IF filter and a second IF filter that receives an output signal from said second mixer;

c) a phase lock loop (PLL) circuit having a first feedback frequency divider that provides a first downconversion signal to said first mixer, said phase lock loop circuit having a second feedback frequency divider that provides a second downconversion signal to said second mixer, said phase lock loop circuit tailored to

multiply the frequency of reference clock in response to a mode signal that indicates whether a GPS wireless signal or a cellular wireless signal is to be received; and

d) a first IF filter tuning and control circuit that tunes and controls a center frequency for said first IF filter and a second IF filter tuning and control circuit that tunes and controls a center frequency for said second IF filter, said first and second IF tuning and control circuits each tailored to use a plurality of reference frequencies for said tuning.

12. The wireless receiver of claim 11 wherein said cellular wireless signal can be an AMPS signal.

13. The wireless receiver of claim 11 wherein said cellular wireless signal can be a CDMA wireless signal.

14. The wireless receiver of claim 11 wherein said cellular wireless signal can be a GSM wireless signal.

15. The wireless receiver of claim 11 further comprising a multiplexer that receives said output signal from said first IF filter at a first input and wherein said multiplexer also receives said output signal from said second IF filter at second input, said multiplexer also receiving said mode input so that:

1) single downconversion is performed when said first input is selected in response to said mode input; and

2) dual downconversion is performed when said second input is selected in response to said mode input.

16. The wireless receiver of claim 15 wherein said mode input is configured such that said single downconversion is performed for reception for said cellular wireless signal and said dual downconversion is performed for said GPS wireless signal.

17. The wireless receiver of claim 11 further comprising a frequency divider that divides the frequency of a master clock signal to provide said reference clock.

18. The wireless receiver of claim 17 wherein said reference clock frequency is less than 1 MHz.

19. The wireless receiver of claim 17 wherein master clock is 13.0 MHz.

20. The wireless receiver of claim 11 wherein said PLL circuit further comprises a third feedback frequency divider.

21. A method, comprising:

a) testing a reference element at a first reference frequency and a second reference frequency, said reference element correlated to a component within an IF filter that can receive either a GPS wireless signal or a cellular wireless signal; and

b) determining, in light of said testing, a change to a GPS nominal value for said IF filter, said GPS nominal value for tailoring a passband of said IF filter to receive said GPS wireless signal if inaccuracies in said passband are undetected by said testing.

22. The method of claim 21 wherein said reference element is a resistor.

23. The method of claim 22 wherein said resistor is part of an inverter structure within a voltage controlled oscillator (VCO).

24. The method of claim 21 wherein said determining further comprises comparing the loop filter output voltage to an expected loop filter output voltage, said loop filter output coupled to an input of a VCO, said loop filter and said VCO within a phase lock loop circuit.

25. The method of claim 21 wherein a first loop filter output voltage results from said first reference frequency being applied to a phase lock loop circuit and a second loop filter output voltage results from said second reference frequency being applied to a phase lock loop circuit.

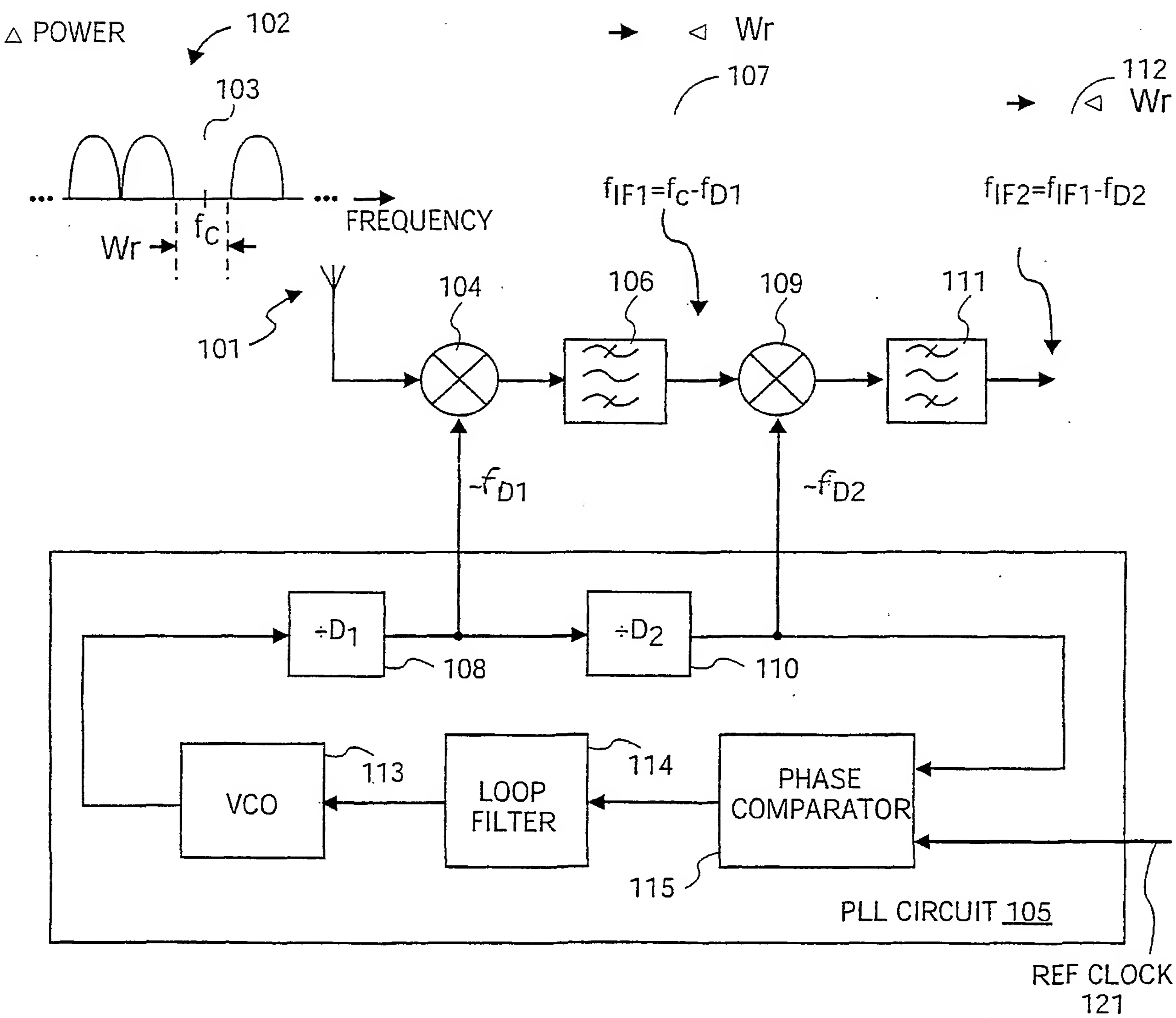
26. The method of claim 25 wherein said first and second loop filter output voltages are both less than a third loop filter output voltage that correlates to said GPS nominal value.

27. The method of claim 25 wherein said first and second loop filter output voltages are both greater than a third loop filter output voltage that correlates to said GPS nominal value.

28. The method of claim 25 wherein a third loop filter output voltage that correlates to said GPS nominal value is between said first and second loop filter output voltages.

29. The method of claim 21 wherein said reference element is a monostable reference element.

30. The method of claim 21 further comprising applying said change to said GPS nominal value.



POWER
102
103
FREQUENCY
Wr
f_C
101
104
106
109
111
107
Wr
112
Wr
$f_{IF1}=f_C-f_{D1}$
$f_{IF2}=f_{IF1}-f_{D2}$
$\sim f_{D1}$
$\sim f_{D2}$
$\div D_1$
108
$\div D_2$
110
VCO
113
LOOP FILTER
114
PHASE COMPARATOR
115
PLL CIRCUIT 105
REF CLOCK 121

FIG. 1

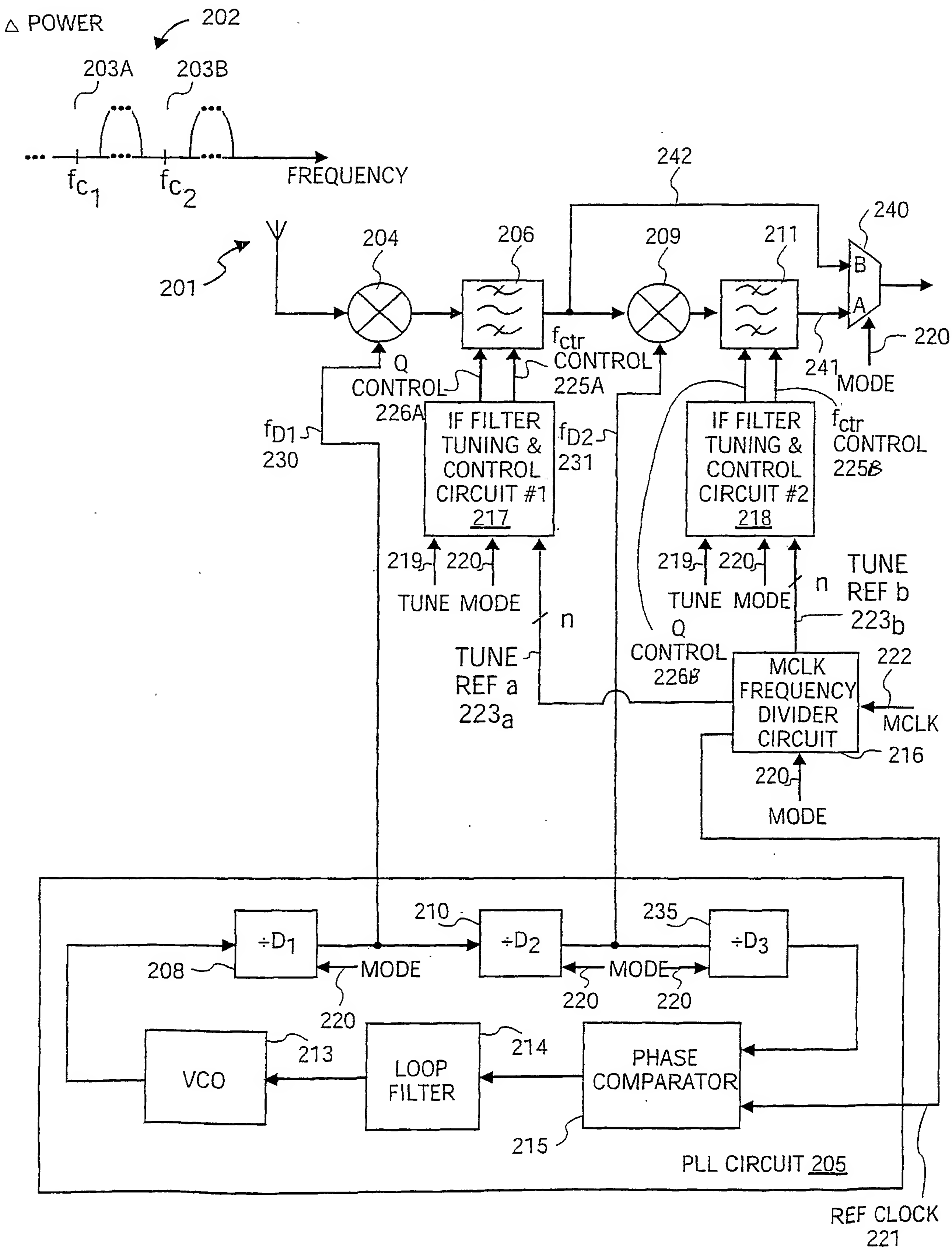

△ POWER
202
203A
203B
f_{c_1}
f_{c_2}
FREQUENCY
201
204
206
209
211
242
240
B
A
220
MODE
241
Q CONTROL 226A
f_{ctr} CONTROL 225A
f_{D1} 230
f_{D2} 231
IF FILTER TUNING & CONTROL CIRCUIT #1 217
IF FILTER TUNING & CONTROL CIRCUIT #2 218
f_{ctr} CONTROL 225B
219
220
TUNE MODE
n
TUNE REF a 223a
Q CONTROL 226B
TUNE REF b 223b
MCLK FREQUENCY DIVIDER CIRCUIT
222
MCLK
216
MODE
÷D1
÷D2
÷D3
208
210
235
VCO
213
LOOP FILTER
214
PHASE COMPARATOR
215
PLL CIRCUIT 205
REF CLOCK 221

FIG. 2

MODE	316a MCLK DIVIDER VALUE	321a REF CLK	305a PLL MULT.	313a VCO FREQ.	308a FIRST DIVIDER VALUE	330a FIRST DOWN CONV. FREQ.	304a FIRST INTERMED. FREQ.	310a SECOND DIVIDER VALUE	331a SECOND DOWN CONV. FREQ.	311a SECOND INTERMED. FREQ.	335a THIRD DIVIDER VALUE
301a GPS	$D3_a$	f_{REFa}	X_a	f_{vcoa}	D_{1a}	f_{D1a}	f_{IF1a}	D_{2a}	f_{D2A}	f_{IF2a}	D_{3a}
302a CELLULAR	$D3_b$	f_{REFb}	X_b	f_{vcob}	D_{1b}	f_{D1b}	f_{IF1b}	D_{2b}	f_{D2B}	f_{IF2b}	D_{3b}

MCLK = Z MHz

FIG. 3A

MODE	316b MCLK DIVIDER VALUE	321b REF CLK (MHz)	305b PLL MULT.	313b VCO FREQ. (MHz)	308b FIRST DIVIDER VALUE	330b FIRST DOWN CONV. FREQ. (MHz)	304b FIRST INTERMED. FREQ. (MHz)	310b SECOND DIVIDER VALUE	331b SECOND DOWN CONV. FREQ. (MHz)	311b SECOND INTERMED. FREQ (MHz)	335b THIRD DIVIDER VALUE
GPS	65.0	0.2	16096	3219.2	2	1609.6	34.2	42.0	38.3	4.1	16096/84
CELLULAR	65.0	0.2	5800	1160	1	1160	270.00	4.3	269.8	0.2	5800/4.3

MCLK = 13.0 MHz

FIG. 3B

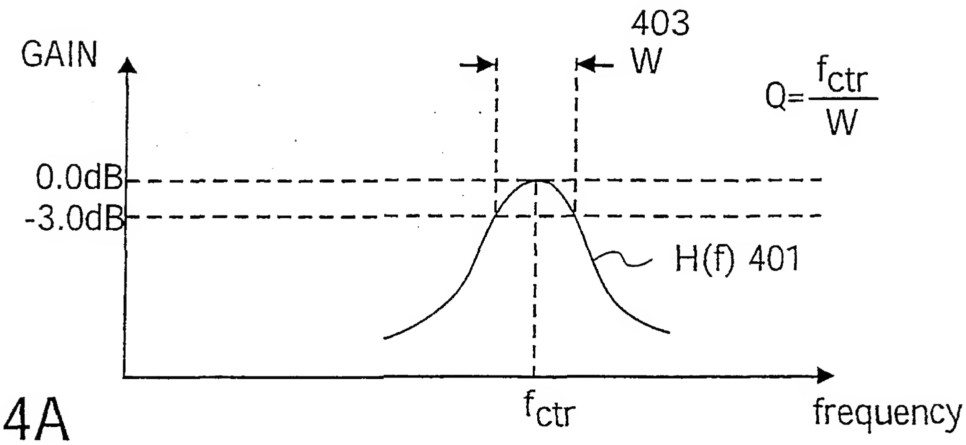
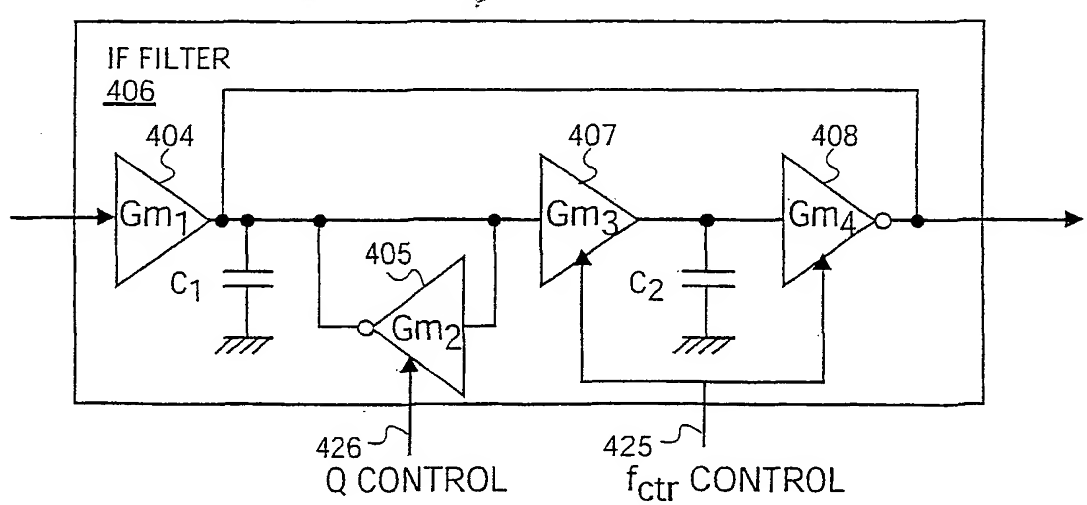


FIG. 4A



$$H(S)=\frac{S\omega_0}{S^2+S\left(\frac{Q}{\omega_0}\right)+\omega_0{}^2}$$

$$\omega_0 = 2\pi F_{ctr} = \sqrt{\frac{Gm_3\ Gm_4}{C_1\ \ C_2}}$$

$$Q=\sqrt{\frac{C_1 Gm_3\ Gm_4}{C_2\ G^2 m_2}}$$

FIG. 4B

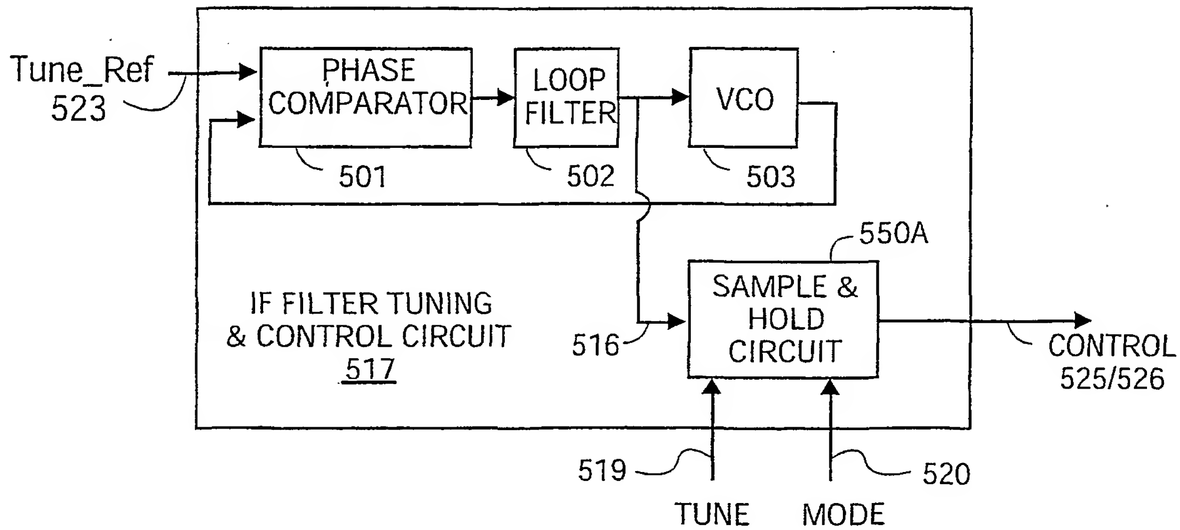

Tune_Ref
523
PHASE COMPARATOR
501
LOOP FILTER
502
VCO
503
550A
SAMPLE & HOLD CIRCUIT
IF FILTER TUNING & CONTROL CIRCUIT 517
516
CONTROL 525/526
519
520
TUNE
MODE

FIG. 5A

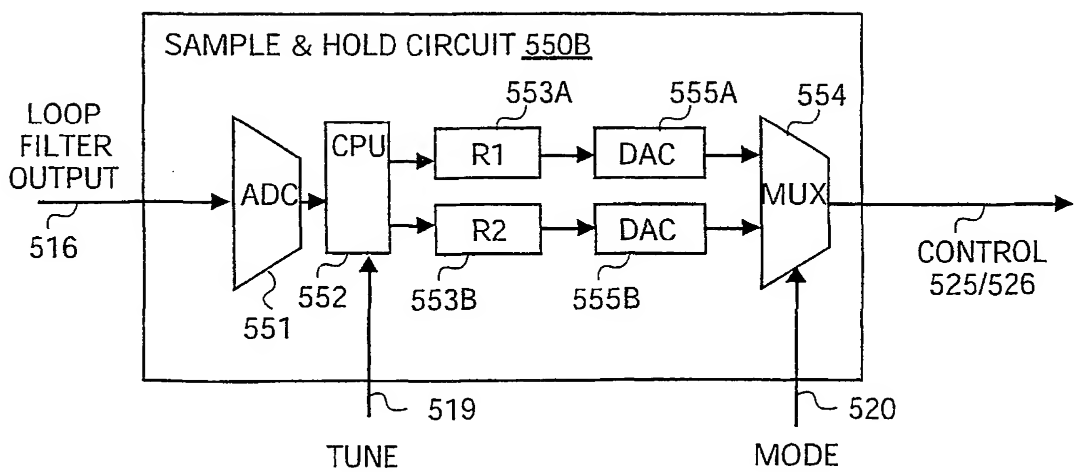

SAMPLE & HOLD CIRCUIT 550B
LOOP FILTER OUTPUT
516
ADC
551
CPU
552
553A
R1
R2
553B
555A
DAC
DAC
555B
554
MUX
CONTROL 525/526
519
TUNE
520
MODE

FIG. 5B

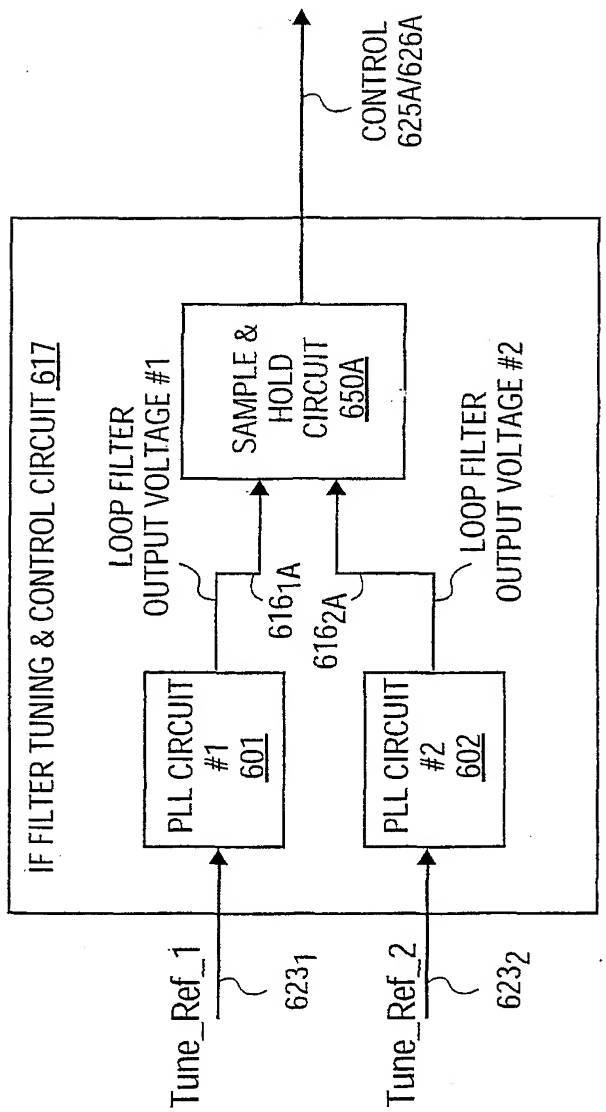

IF FILTER TUNING & CONTROL CIRCUIT 617
Tune_Ref_1
623_1
Tune_Ref_2
623_2
PLL CIRCUIT #1 601
PLL CIRCUIT #2 602
LOOP FILTER OUTPUT VOLTAGE #1
LOOP FILTER OUTPUT VOLTAGE #2
616_{1A}
616_{2A}
SAMPLE & HOLD CIRCUIT 650A
CONTROL 625A/626A

FIG. 6A

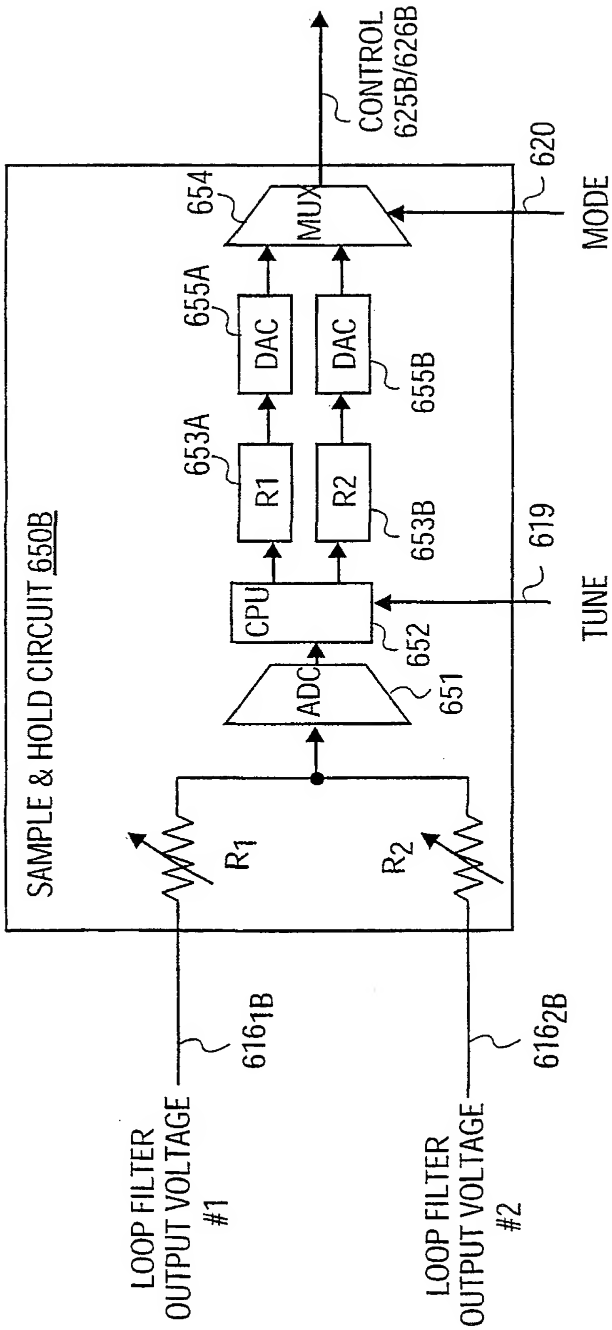

SAMPLE & HOLD CIRCUIT 650B
LOOP FILTER OUTPUT VOLTAGE #1
LOOP FILTER OUTPUT VOLTAGE #2
616₁B
616₂B
R1
R2
ADC
651
CPU
652
TUNE
619
R1
R2
653A
653B
DAC
DAC
655A
655B
MUX
654
MODE
620
CONTROL 625B/626B

FIG. 6B

11

PATENT COOPERATION TREATY

PCT

REC'D 10 JUL 2002

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INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PD/47330	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/GB 01/ 05101	International filing date *(day/month/year)* 19/11/2001	(Earliest) Priority Date *(day/month/year)* 23/01/2001
Applicant PARTHUS IRELAND LIMITED		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

      [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

      [ ] contained in the international application in written form.
      [ ] filed together with the international application in computer readable form.
      [ ] furnished subsequently to this Authority in written form.
      [ ] furnished subsequently to this Authority in computer readble form.
      [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
      [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title**,

   [ ] the text is approved as submitted by the applicant.
   [X] the text has been established by this Authority to read as follows:

   A GPS AND CELLULAR RECEIVER AND A METHOD FOR TUNING AND CONTROLLING ITS IF FILT ER

5. With regard to the **abstract**,

   [X] the text is approved as submitted by the applicant.
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 2

   [X] as suggested by the applicant.
   [ ] because the applicant failed to suggest a figure.
   [ ] because this figure better characterizes the invention.
   [ ] None of the figures.

BNSDOCID: <WO_______02060058A1_I_>

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 01/05101

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03J1/00 H03J3/08 H04Q7/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03J H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 002 363 A (KRASNER NORMAN F) 14 December 1999 (1999-12-14) column 5, line 40 -column 6, line 29; figure 1B column 14, line 62; figure 7A	1,2,5,6, 11,12
A	US 6 122 506 A (LAU CHUNG Y ET AL) 19 September 2000 (2000-09-19) abstract; figure 1	1,4-6, 11,14,21

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 May 2002	11/07/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Peeters, M

Form PCT/ISA/210 (second sheet) (July 1992)

BNSDOCID: <WO_______02060058A1_I_>

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	BOEHM K ET AL: "An IF digitizing receiver for a combined GPS/GSM terminal" RADIO AND WIRELESS CONFERENCE, 1998. RAWCON 98. 1998 IEEE COLORADO SPRINGS, CO, USA 9-12 AUG. 1998, NEW YORK, NY, USA, IEEE, US, 9 August 1998 (1998-08-09), pages 39-42, XP010296327 ISBN: 0-7803-4988-1 figure 1	1,4,5, 11, 14-16,21
A	US 6 097 974 A (CAMP JR WILLIAM O ET AL) 1 August 2000 (2000-08-01) abstract; figure 9	1,3,5, 11,13,15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 01/05101

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 5874914 A	23-02-1999
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